CLAIMS

What is Claimed is:

1. A delay circuit comprising:

a delay element comprising:

a first switching leg comprising a first switched capacitor receiving a clock signal; and

a second switching leg comprising a second switched capacitor receiving a clock signal;

an input signal switching leg coupled with said delay element, said input signal switching leg providing a signal input to said delay element; and

a delay inverter coupled with said delay element, wherein a propagation delay of said delay circuit is a function of a ratio between a switched capacitance of said delay element and an input capacitance to said delay inverter.

2. The circuit of Claim 1 wherein said first switching leg is a negative channel metal-oxide semiconductor (NMOS) switching leg.

3. The circuit of Claim 1 wherein said second switching leg is a positive channel metal-oxide semiconductor (PMOS) switching leg.

4. The circuit of Claim 1 wherein said delay element further comprises a trip inverter coupled with said first switching leg and said second switching leg.

5. The circuit of Claim 4 wherein said first switching leg further comprises:

a first operational transconductance amplifier (OTA) coupled with said trip inverter and a NMOS transistor; and

a first hold capacitor coupled with said first OTA and said first switched capacitor for supplying voltage to said first switched capacitor.

6. The circuit of Claim 4 wherein said second switching leg further comprises:

a second operational transconductance amplifier (OTA) coupled with said trip inverter and a PMOS transistor; and

a second hold capacitor coupled with said second OTA and said second switched capacitor for supplying voltage to said second switched capacitor.

7. The circuit of Claim 1 wherein said first and second switched capacitors further comprise a first and second clock-controlled switch for driving said switched capacitor.

8. The circuit of Claim 7 wherein the propagation delay of the delay circuit is proportional to the clock signal frequency.

9. A delay circuit comprising:

a delay element comprising:

a negative channel metal-oxide semiconductor (NMOS) switching leg comprising a first switched capacitor receiving a clock signal; and

a positive channel metal-oxide semiconductor (PMOS) switching leg comprising a second switched capacitor receiving a clock signal;

an input signal switching leg coupled with an input of said delay element; and

a delay inverter coupled with an output from said delay element, wherein a propagation delay of said delay circuit is proportional to said clock signal frequency.

10. The circuit of Claim 9 wherein said delay element further comprises a trip inverter having a trip voltage coupled with said NMOS switching leg and said PMOS switching leg.

11. The circuit of Claim 9 wherein said NMOS switching leg further comprises:

a first operational transconductance amplifier (OTA) coupled with said trip inverter and a first NMOS transistor;

a first hold capacitor coupled with said first OTA and said first switched capacitor;

a second NMOS transistor coupled with a source and said switched capacitor; and

a third NMOS transistor coupled with said first NMOS transistor and said input signal switching leg.

12. The circuit of Claim 9 wherein said PMOS switching leg further comprises:

a second operational transconductance amplifier (OTA) coupled with said trip inverter and a first PMOS transistor; and

a second hold capacitor coupled with said second OTA and said second switched capacitor for supplying voltage to said second switched capacitor;

a second PMOS transistor coupled with a source and said switched capacitor; and

a third PMOS transistor coupled with said first PMOS transistor and said input signal switching leg.

13. The circuit of Claim 9 wherein the propagation delay of the delay circuit is a function of a ratio of an input capacitance and a switched capacitance.

14. The circuit of Claim 9 wherein the propagation delay of the delay element is scaleable with respect to the frequency of the clock signal using an external control pin.

15. A memory system for delaying a clock signal with respect to a data clock signal comprising:

a memory device for outputting data in conjunction with a clock signal; and

a delay circuit utilizing a switched capacitor to provide a propagation delay, wherein the delay element skews the clock signal versus data output from said memory element, and wherein the propagation delay of said delay circuit is a function of a ratio of an input capacitance and a switched capacitance.

16. The memory system of Claim 15 wherein the propagation delay of said delay circuit is proportional to a frequency of said clock signal.

17. The memory system of Claim 15 wherein the clock signal goes through the delay circuit and the data output does not go through the delay circuit.

18. The memory system of Claim 15 wherein said delay circuit comprises:

a negative channel metal-oxide semiconductor (NMOS) switching leg comprising:

a first operational transconductance amplifier (OTA) coupled with said trip inverter and a first NMOS transistor;

a first hold capacitor coupled with said first OTA and said first switched capacitor;

a second NMOS transistor coupled with a source and said switched capacitor; and

a third NMOS transistor coupled with said first NMOS transistor and said input signal switching leg; and

a positive channel metal-oxide semiconductor (PMOS) switching leg comprising:

a second operational transconductance amplifier (OTA) coupled with said trip inverter and a first PMOS transistor; and

a second hold capacitor coupled with said second OTA and said second switched capacitor for supplying voltage to said second switched capacitor;

a second PMOS transistor coupled with a source and said switched capacitor; and

a third PMOS transistor coupled with said first PMOS transistor and said input signal switching leg.

19. The memory system of Claim 18 wherein the propagation delay of the delay circuit can be controlled by adjusting a ratio of a channel width of said NMOS transistors.

20. The memory system of Claim 18 wherein the propagation delay of the delay circuit can be controlled by adjusting a ratio of a channel width of said PMOS transistors.